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NONVOLATILE SRAM MEMORY CELL

PRIORITY CLAIM

The present application claims priority from French Application for Patent No. 02 16558 filed December 23, 2002, the disclosure of which is hereby incorporated by reference.

BACKGROUND OF THE INVENTION

Technical Field of the Invention

[1] The present invention relates to static random access memories (SRAM) embodied in MOS technology.

Description of Related Art

[2] As is known, a conventional SRAM memory cell comprises six MOS transistors arranged in such a way as to form first and second inverters interconnected between first and second data nodes.

[3] Each inverter comprises a PMOS load transistor connected in series with an NMOS inverter transistor between a DC voltage supply source (DC reference) and a ground reference. The gates of the PMOS and NMOS transistors of each inverter are joined. The common electrodes shared by the NMOS and PMOS transistors constitute a data node.

[4] Two NMOS select transistors provide for the interconnection of the cell with a word line and a bit line, and thus allow reading of the memory point or modification of the latter.

[5] Such cells are advantageous in so far as they are relatively fast. Specifically, the cycle time, that is to say the minimum time between two successive operations of the memory, be it while reading or writing, corresponds to the memory access time, that is to say the time between the moment at which the address is present and the moment at which the item of data read is available at the output of the memory.

[6] However, with this type of memory, the memory is permanent as long as the circuits are powered. Stated otherwise, the data are lost when the memory is no longer powered.

[7] It is therefore necessary to couple these memories to additional nonvolatile memories to which the data are transferred before the power supply is cut off.

[8] In view of the foregoing, there is a need for a nonvolatile SRAM memory cell, that is to say one which is capable of permanently retaining its content.

SUMMARY OF THE INVENTION

[9] An SRAM memory cell comprising first and second inverters interconnected between first and second data nodes, wherein each inverter includes complementary MOS transistors connected in series between a DC reference and a ground reference.

[10] This cell comprises, according to a general characteristic, means for programming the MOS transistors adapted for causing, after programming, an irreversible degradation of a gate oxide layer of at least some of the transistors.

[11] It has thus been noted that such a degradation brings about a modification of the characteristics of the transistors, engendering a drop in the drain current of possibly up to around 30%. Such a degradation is then used for the storage of information, for a duration of retention of possibly up to some ten years.

[12] According to another characteristic of this cell, each inverter comprises a first PMOS transistor and a second NMOS transistor coupled in series between the DC reference and the ground reference, the data nodes being formed respectively between the two NMOS and PMOS transistors of the inverters.

[13] According to yet another characteristic of the SRAM memory cell of the invention, the degraded MOS transistor is a thin gate oxide layer transistor, also known as a GO1 transistor.

[14] After programming, the oxide layer is degraded at least locally in such a way as to obtain, during the reading of the cell, a variation in the current delivered by the transistor.

[15] According to one embodiment, the programming means comprise, for each inverter, a programming transistor linked between a programming control line and the transistors of the inverter.

[16] These programming means thus, for example, comprise an NMOS transistor ensuring the selective linking of the gate of a transistor to be degraded to a programming voltage source delivering a voltage level able to cause, jointly with the DC reference linked to the drain of the said transistor, a degradation in the gate oxide layer of the transistor, the programming transistor being driven by the programming control line.

[17] Furthermore, according to another characteristic, this cell comprises means for causing the cell to operate as an SRAM memory after programming.

[18] These means may be embodied in the form of NMOS transistors providing for the interconnection of the inverters, these transistors being linked to a control line for instructing the cell to operate as an SRAM memory.

[19] The drain electrode and source electrode of each of these NMOS transistors are respectively linked to the gate of the transistors of one of the inverters.

BRIEF DESCRIPTION OF THE DRAWINGS

[20] A more complete understanding of the method and apparatus of the present invention may be acquired by reference to the following Detailed Description when taken in conjunction with the accompanying Drawings wherein:

[21] FIGURE 1 is a diagram illustrating the structure of a static, nonvolatile, SRAM memory cell according to the invention; and

[22] FIGURE 2 shows the profile of control signals applied to the cell of Figure 1.

DETAILED DESCRIPTION OF THE DRAWINGS

[23] Represented in Figure 1 is the general structure of a nonvolatile SRAM cell, in accordance with the invention, designated by the general numerical reference 10.

[24] As may be seen in this figure, this SRAM memory cell 10 is embodied on the basis of an SRAM memory structure point 12 (of the common 6T type) that behaves in a conventional manner. The memory cell 10 is supplemented in such a way as to make it possible to cause a degradation of one or more of the transistors involved in the constitution of the memory point 12 during the programming of the cell 10, in such a way as to cause an irreversible degradation of these transistors such that it causes a decrease in the current delivered by these transistors during reading and decrease in the threshold voltage.

[25] As may be seen in this Figure 1, the SRAM memory point 12 is constituted by an association of two interconnected inverters 14 and 16.

[26] More particularly, each inverter 14 and 16 is constituted by the series association of a first PMOS load transistor, respectively 18 and 18' and of a second NMOS inverter transistor, respectively 20 and 20', linked in series between a DC voltage supply source (reference) VDD and a ground reference 22.

[27] The transistors are arranged so that the drain D of each of the first PMOS load transistors 18 and 18' is linked to the supply source VDD and that their sources S are linked to the drains D of the second NMOS inverter transistors 20 and 20' of the same inverter and to the gate G of the second NMOS inverter transistor 20 of the other inverter.

[28] Two additional select transistors 24 and 26, which allow access to the data nodes N1 and N2 of the SRAM memory cell which are formed at the level of the interconnection of the first and second transistors 18, 18' and 20, 20', respectively, of each inverter 14 and 16, are controlled by a word line WL for transferring a stored bit to bit lines BL and BL B.

[29] For the programming of the SRAM cell 10, the latter is provided with programming transistors 28 and 30, constituted by NMOS transistors placed in series between the gates G of the first PMOS transistors 18, 18' of the inverters 14 and 16.

[30] These transistors 28 and 30 are controlled by a programming control line PROG, the gate of each of these transistors being connected to this control line PROG. Moreover, the drain electrode and source electrode of these control transistors are respectively linked to a second DC voltage supply source VREF intended for setting the gate of the first transistors 18 to a level allowing a degradation of the gate oxide. Likewise, the voltage VDD provided by the first DC voltage supply source is chosen in such a way as to create a voltage VDS between the source and the drain of these first transistors 18/18' that is able to cause a degradation of the gate oxide layer of these transistors.

[31] For the embodiment of the first transistors 18, 18' of each of the inverters 14 and 16, use is made of an MOS transistor of thin gate oxide type, also known by the name "GO1

MOS transistor". All the other transistors are thick oxide transistors so as not to be affected by the programming stress.

[32] With such transistors, for example, in order to cause a degradation of the gate oxide layer, one uses a voltage VDD of the order of 3.3 volts and a voltage VREF of the order of 2 volts. Under these conditions, a local degradation of the gate oxide layer is created on the drain zone side of these transistors, this bringing about a drop in the threshold voltage of these transistors as well as a drop in the drain current. Such a drop in current may reach a value of 30%, depending on the reading conditions. For example, a reduction in the current of 22% is achieved for a gate voltage of 1.2 volts and a drain voltage of 1.2 volts. A reduction in current of 30% is achieved for a gate voltage of 1.2 volts and a drain voltage of 0.1 volt.

[33] Finally, it is seen in Figure 1 that the first and second transistors 18 and 20 of each inverter are interconnected by way of additional NMOS transistors 32 and 34 arranged so that their gate G is linked to an SRAM line for controlling the operation of the cell as an SRAM memory and that their drain and their source are respectively connected to the gate of the first and second transistors 18 and 20. Thus, a high level on this SRAM control line causes the linking of the gate G of the transistors of the inverters 14 and 16.

[34] The profile of the voltage levels available on the lines VDD, VREF, PROG and SRAM will now be described with reference to Figure 2.

[35] As indicated previously, during a cycle I of operation of the cell 10 as an SRAM memory, the voltage available on the SRAM line is set to a high level, for example of the order of 1.2 volts. The voltage levels on the lines VREF and PROG are set to a low level and the

voltage VDD delivered by the first voltage supply source is set to a low level, for example 1.2 volts.

[36] To carry out a cycle for entering a data item to be programmed, this data item "DATA" is set on the bit lines BL and BL B, that is to say (0-1) or (1-0). Next, the word line WL goes to the high state so as to set the memory point. The word line WL then goes to the low state. The bit lines BL and BL B can then change state in such a way as to write the other cells set on the same bit lines.

[37] To cause the programming of the cell, the voltage on the SRAM line is zeroed and the voltage supplied by the PROG and VREF lines is raised to a level of the order of 1 volt, for example 1.2 volts for the voltage on the PROG line and 1 volt for the VREF line (cycle II). Finally, to proceed to the actual programming (cycle III), the voltage on the PROG line and the voltage delivered by the first supply source VDD are raised to a level of 3.3 volts. As far as the voltage VREF delivered by the second voltage supply source is concerned, the latter is for example adjusted to a level of 2.2 volts.

[38] Such voltage levels bring about, as indicated previously, an irreversible degradation of the transistors 18 and 18', which degradation can be used for the storage of an information item for a duration of possibly up to some ten years.

[39] On power-up, the nodes N1 and N2 are at 0 V. Depending on the data item programmed previously, one of the MOS transistors 18 or 18' provides less current than the other MOS 18' or 18. The node N2 is initialized to 1 and N1 to 0 V, or N2 to 0 V and N1 to 1, during the rise in the power supply. During reading, the bit line WL and the PROG signal are at

0. The SRAM signal must be 1 before the rise in VDD. Finally, the data item is set on the bit lines BL and BL B.

[40] It will be noted finally that the transistors 28 and 30 of the programming means may be replaced with diodes or diode-configured transistors.

[41] Although preferred embodiments of the method and apparatus of the present invention have been illustrated in the accompanying Drawings and described in the foregoing Detailed Description, it will be understood that the invention is not limited to the embodiments disclosed, but is capable of numerous rearrangements, modifications and substitutions without departing from the spirit of the invention as set forth and defined by the following claims.